

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 3 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DESCRIPTION/ORDERING INFORMATION

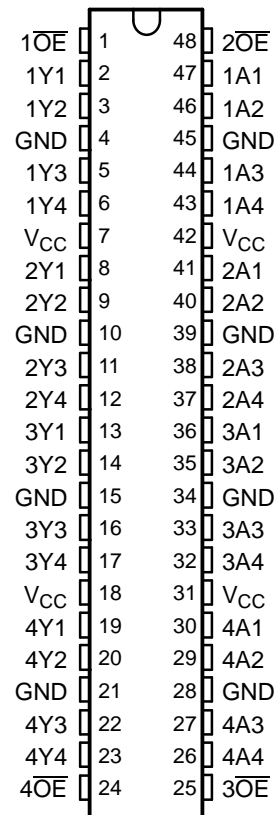
This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16244 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|-----------------------|-----------------------|------------------|
| –40°C to 85°C | FBGA – GRD | Tape and reel | SN74ALVCH16244GRDR | VH244 |
| | FBGA – ZRD (Pb-free) | | SN74ALVCH16244ZRDR | |
| | SSOP – DL | Tube | SN74ALVCH16244DL | ALVCH16244 |
| | | Tape and reel | SN74ALVCH16244DLR | |
| | TSSOP – DGG | Tape and reel | SN74ALVCH16244DGGR | ALVCH16244 |
| | | | 74ALVCH16244DGGRE4 | |
| | TVSOP – DGV | Tape and reel | SN74ALVCH16244DGVR | VH244 |
| | | | 74ALVCH16244DGVRE4 | |
| VFBGA – GQL | Tape and reel | SN74ALVCH16244KR | VH244 | |
| | | VFBGA – ZQL (Pb-free) | | 74ALVCH16244ZQLR |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

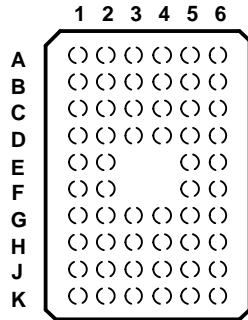
SN74ALVCH16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES014K—JULY 1995—REVISED OCTOBER 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

GQL OR ZQL PACKAGE
(TOP VIEW)

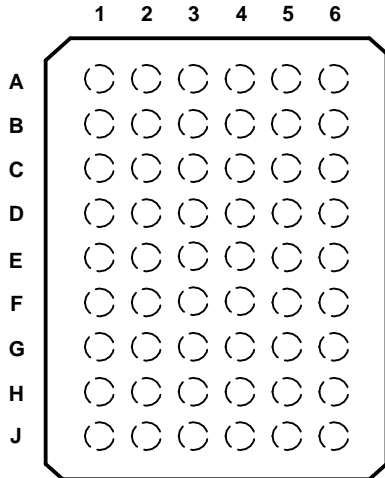


TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------------------|-----|----------|----------|-----|------------------|
| A | $\overline{1OE}$ | NC | NC | NC | NC | $2\overline{OE}$ |
| B | 1Y2 | 1Y1 | GND | GND | 1A1 | 1A2 |
| C | 1Y4 | 1Y3 | V_{CC} | V_{CC} | 1A3 | 1A4 |
| D | 2Y2 | 2Y1 | GND | GND | 2A1 | 2A2 |
| E | 2Y4 | 2Y3 | | | 2A3 | 2A4 |
| F | 3Y1 | 3Y2 | | | 3A2 | 3A1 |
| G | 3Y3 | 3Y4 | GND | GND | 3A4 | 3A3 |
| H | 4Y1 | 4Y2 | V_{CC} | V_{CC} | 4A2 | 4A1 |
| J | 4Y3 | 4Y4 | GND | GND | 4A4 | 4A3 |
| K | $4\overline{OE}$ | NC | NC | NC | NC | $3\overline{OE}$ |

(1) NC – No internal connection

GRD OR ZRD PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)

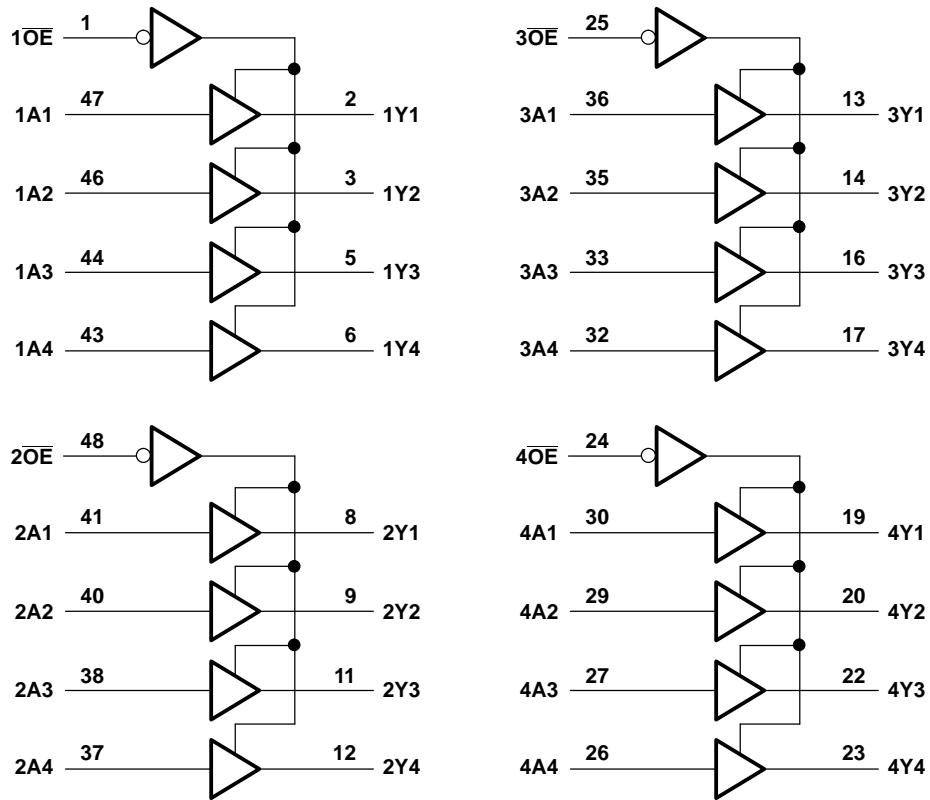
| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|------------------|------------------|-----|-----|
| A | 1Y1 | NC | $1\overline{OE}$ | $2\overline{OE}$ | NC | 1A1 |
| B | 1Y3 | 1Y2 | NC | NC | 1A2 | 1A3 |
| C | 2Y1 | 1Y4 | V_{CC} | V_{CC} | 1A4 | 2A1 |
| D | 2Y3 | 2Y2 | GND | GND | 2A2 | 2A3 |
| E | 3Y1 | 2Y4 | GND | GND | 2A4 | 3A1 |
| F | 3Y3 | 3Y2 | GND | GND | 3A2 | 3A3 |
| G | 4Y1 | 3Y4 | V_{CC} | V_{CC} | 3A4 | 4A1 |
| H | 4Y3 | 4Y2 | NC | NC | 4A2 | 4A3 |
| J | 4Y4 | NC | $4\overline{OE}$ | $3\overline{OE}$ | NC | 4A4 |

(1) NC – No internal connection

FUNCTION TABLE
(EACH 4-BIT BUFFER)

| INPUTS | | OUTPUT Y |
|-----------------|---|-------------|
| \overline{OE} | A | |
| L | H | H |
| L | L | L |
| H | X | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, and DL packages.

SN74ALVCH16244

16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCES014K–JULY 1995–REVISED OCTOBER 2005

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-----------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 4.6 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 4.6 | V |
| V_O | Output voltage range ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through each V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | 70 | °C/W |
| | | DGV package | 58 | |
| | | DL package | 63 | |
| | | GQL/ZQL package | 42 | |
| | | GRD/ZRD package | 36 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---|----------------------|------|
| V_{CC} | Supply voltage | 1.65 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.65 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 0.7 | |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 0.8 | |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 1.65\text{ V}$ | -4 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | -12 | |
| | | $V_{CC} = 2.7\text{ V}$ | -12 | |
| | | $V_{CC} = 3\text{ V}$ | -24 | |
| I_{OL} | Low-level output current | $V_{CC} = 1.65\text{ V}$ | 4 | mA |
| | | $V_{CC} = 2.3\text{ V}$ | 12 | |
| | | $V_{CC} = 2.7\text{ V}$ | 12 | |
| | | $V_{CC} = 3\text{ V}$ | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|-------------------------|--|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | | I _{OH} = –100 μA | 1.65 V to 3.6 V | V _{CC} – 0.2 | | | V |
| | | I _{OH} = –4 mA | 1.65 V | 1.2 | | | |
| | | I _{OH} = –6 mA | 2.3 V | 2 | | | |
| | | I _{OH} = –12 mA | 2.3 V | 1.7 | | | |
| | | | 2.7 V | 2.2 | | | |
| | | I _{OH} = –24 mA | 3 V | 2.4 | | | |
| V _{OL} | | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | 0.2 | V |
| | | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | | I _{OL} = 6 mA | 2.3 V | | | 0.4 | |
| | | I _{OL} = 12 mA | 2.3 V | | | 0.7 | |
| | | | 2.7 V | | | 0.4 | |
| | I _{OL} = 24 mA | 3 V | | | 0.55 | | |
| I _I | | V _I = V _{CC} or GND | 3.6 V | | | ±5 | μA |
| I _{I(hold)} | | V _I = 0.58 V | 1.65 V | 25 | | | μA |
| | | V _I = 1.07 V | 1.65 V | –25 | | | |
| | | V _I = 0.7 V | 2.3 V | 45 | | | |
| | | V _I = 1.7 V | 2.3 V | –45 | | | |
| | | V _I = 0.8 V | 3 V | 75 | | | |
| | | V _I = 2 V | 3 V | –75 | | | |
| | | V _I = 0 to 3.6 V ⁽²⁾ | 3.6 V | | | ±500 | |
| I _{OZ} | | V _O = V _{CC} or GND | 3.6 V | | | ±10 | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | | 40 | μA |
| ΔI _{CC} | | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 3 V to 3.6 V | | | 750 | μA |
| C _i | Control inputs | V _I = V _{CC} or GND | 3.3 V | 3 | | | pF |
| | Data inputs | | | 6 | | | |
| C _o | Outputs | V _O = V _{CC} or GND | 3.3 V | 7 | | | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|------------------|--------------|-------------|-------------------------|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | (1) | 1 | 3.7 | 3.6 | | 1 | 3 | ns |
| t _{en} | OE | Y | (1) | 1 | 5.7 | 5.4 | | 1 | 4.4 | ns |
| t _{dis} | OE | Y | (1) | 1 | 5.2 | 4.6 | | 1 | 4.1 | ns |

(1) This information was not available at the time of publication.

SN74ALVCH16244
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCES014K–JULY 1995–REVISED OCTOBER 2005

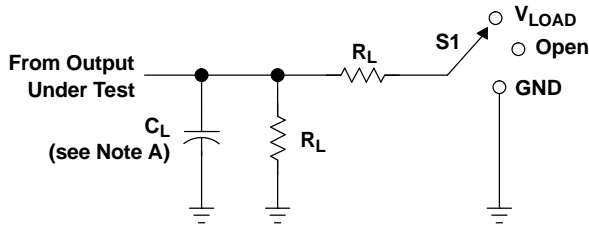
Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|-----------|-------------------------------|------------------|-------------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance | Outputs enabled | (1) | 16 | 19 | pF |
| | | Outputs disabled | (1) | 4 | 5 | |

(1) This information was not available at the time of publication.

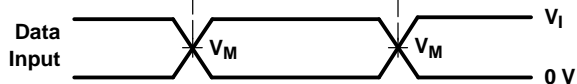
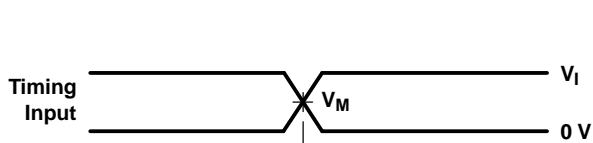
PARAMETER MEASUREMENT INFORMATION



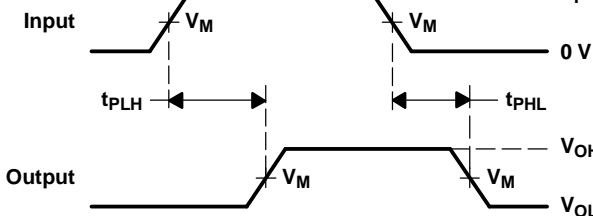
| TEST | S1 |
|-------------------|------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

LOAD CIRCUIT

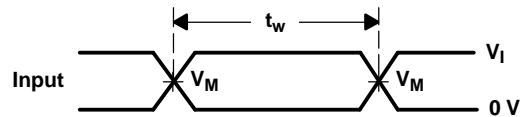
| V_{CC} | INPUT | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|-------------------|----------|---------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| 1.8 V | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5 V \pm 0.2 V$ | V_{CC} | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3 V \pm 0.3 V$ | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



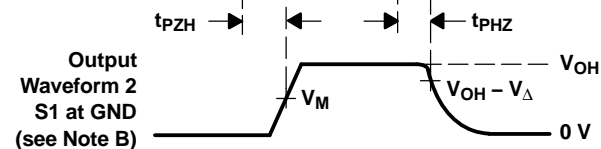
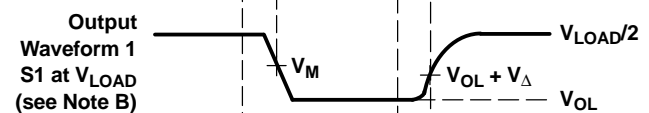
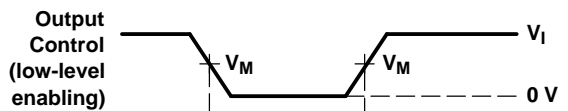
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|----------------------------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74ALVCH16244DGGRE4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH16244DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH16244DGVRE4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH16244DGVRG4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH16244DLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH16244DLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH16244GRDR | ACTIVE | BGA MI CROSTA R JUNI OR | GRD | 54 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| 74ALVCH16244ZQLR | ACTIVE | BGA MI CROSTA R JUNI OR | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| 74ALVCH16244ZRDR | ACTIVE | BGA MI CROSTA R JUNI OR | ZRD | 54 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| SN74ALVCH16244DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH16244DGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH16244DL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH16244DLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH16244KR | NRND | BGA MI CROSTA R JUNI OR | GQL | 56 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



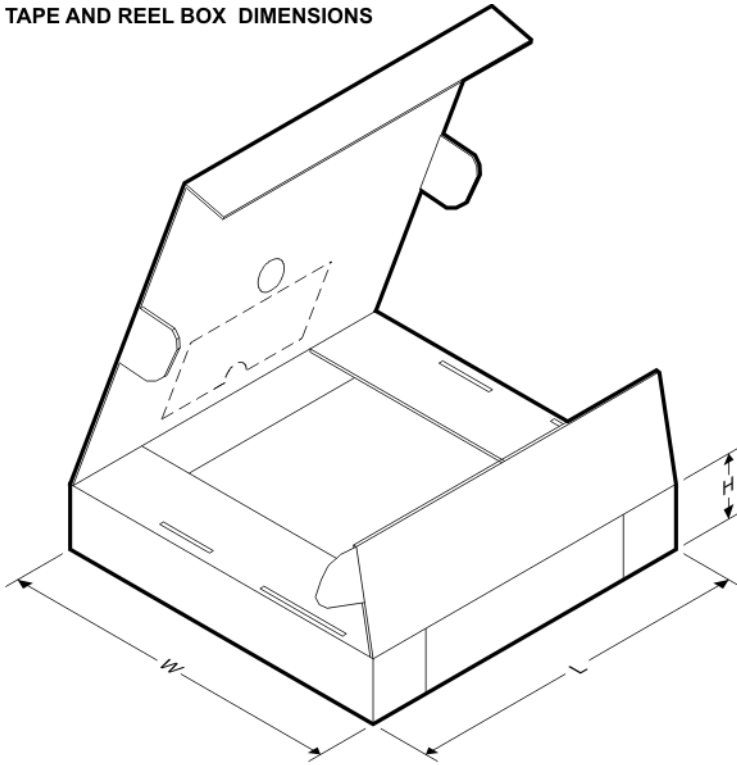
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74ALVCH16244GRDR | BGA MICROSTAR JUNIOR | GRD | 54 | 1000 | 330.0 | 16.4 | 5.8 | 8.3 | 1.55 | 8.0 | 16.0 | Q1 |
| 74ALVCH16244ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.45 | 8.0 | 16.0 | Q1 |
| 74ALVCH16244ZRDR | BGA MICROSTAR JUNIOR | ZRD | 54 | 1000 | 330.0 | 16.4 | 5.8 | 8.3 | 1.55 | 8.0 | 16.0 | Q1 |
| SN74ALVCH16244DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74ALVCH16244DGVR | TVSOP | DGV | 48 | 2000 | 330.0 | 24.4 | 6.8 | 10.1 | 1.6 | 12.0 | 24.0 | Q1 |
| SN74ALVCH16244DLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74ALVCH16244KR | BGA MICROSTAR JUNIOR | GQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.45 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

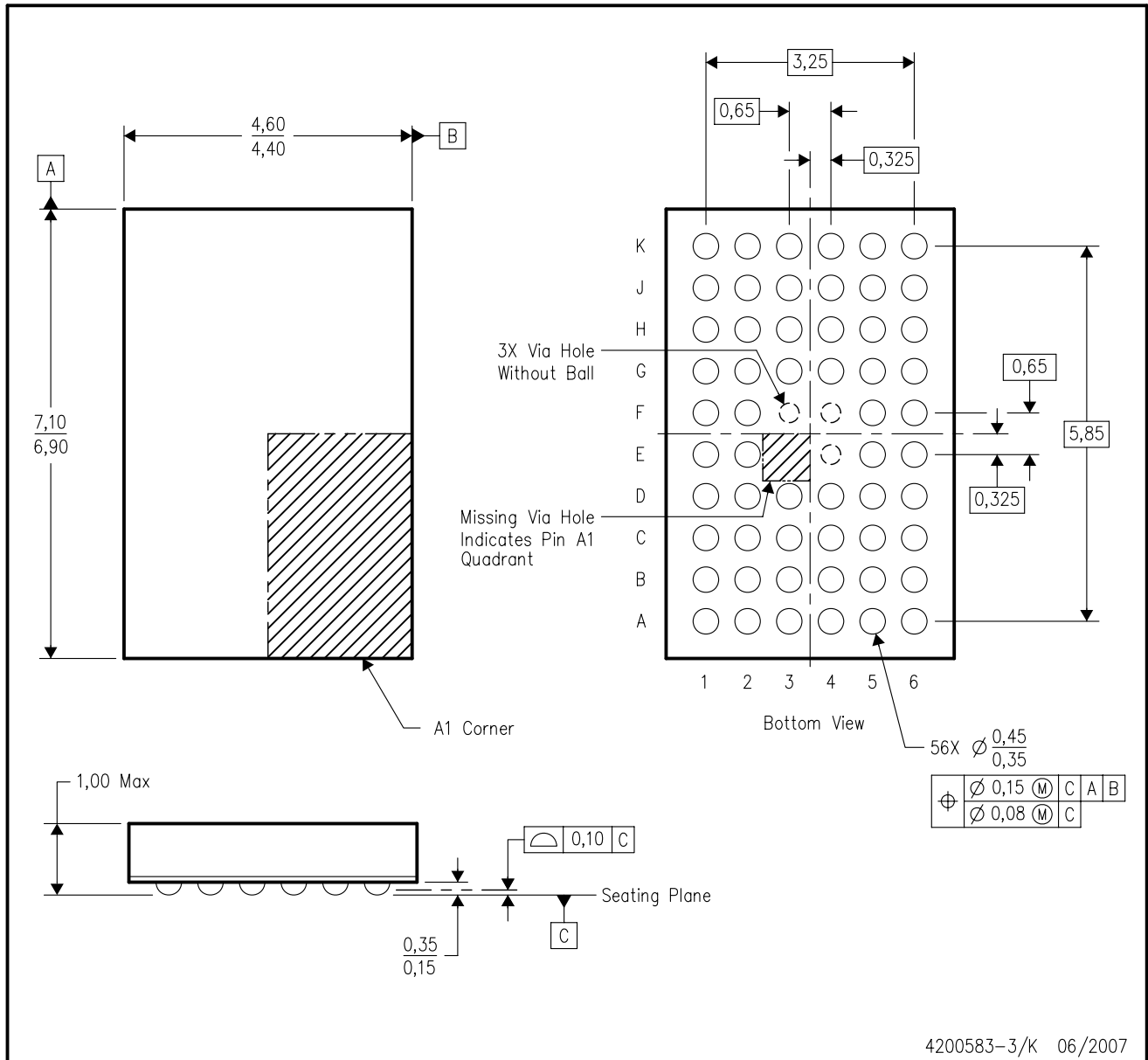


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| 74ALVCH16244GRDR | BGA MICROSTAR JUNIOR | GRD | 54 | 1000 | 346.0 | 346.0 | 33.0 |
| 74ALVCH16244ZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 346.0 | 346.0 | 33.0 |
| 74ALVCH16244ZRDR | BGA MICROSTAR JUNIOR | ZRD | 54 | 1000 | 346.0 | 346.0 | 33.0 |
| SN74ALVCH16244DGGR | TSSOP | DGG | 48 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ALVCH16244DGVR | TVSOP | DGV | 48 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ALVCH16244DLR | SSOP | DL | 48 | 1000 | 346.0 | 346.0 | 49.0 |
| SN74ALVCH16244KR | BGA MICROSTAR JUNIOR | GQL | 56 | 1000 | 346.0 | 346.0 | 33.0 |

GQL (R-PBGA-N56)

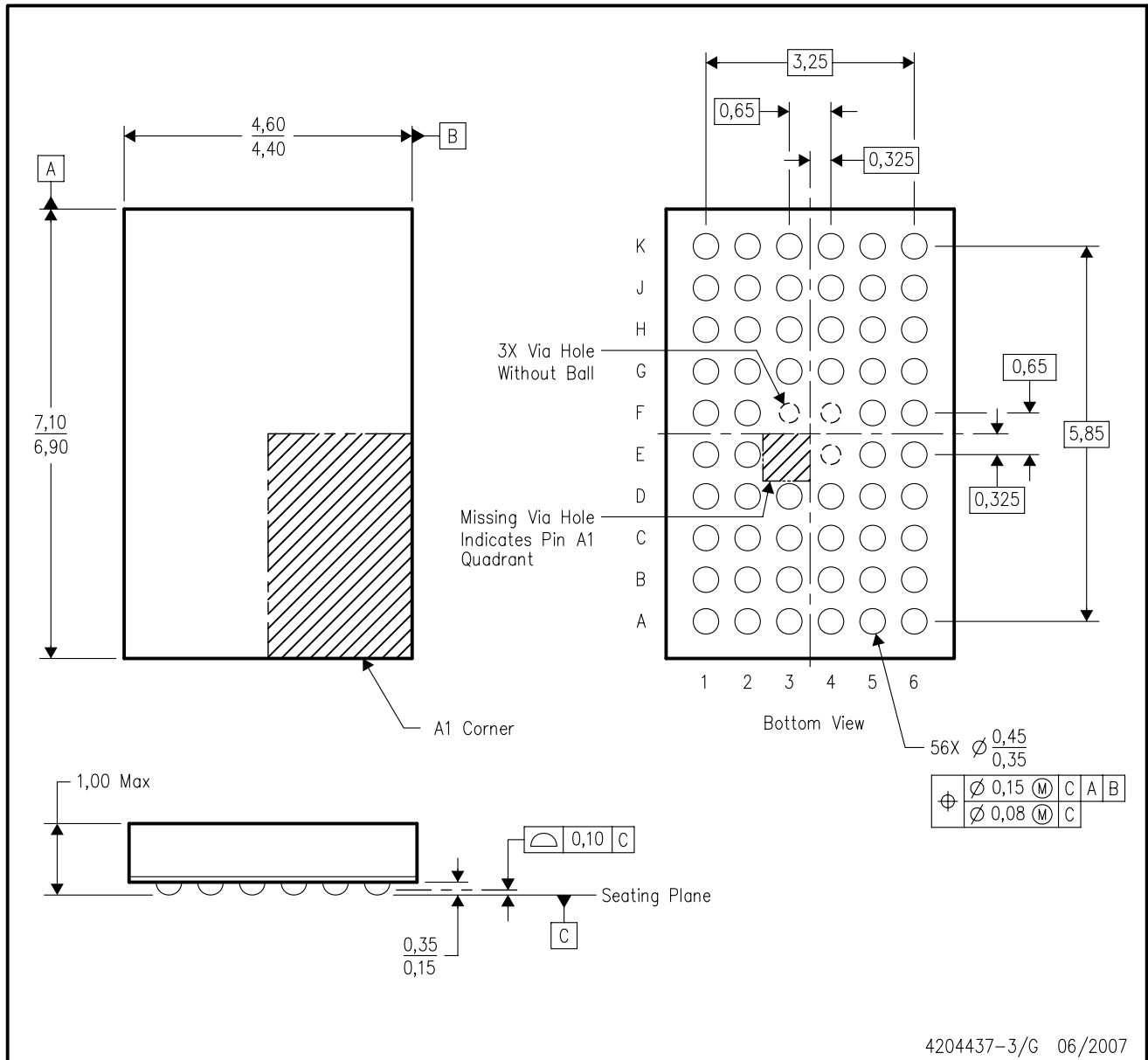
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

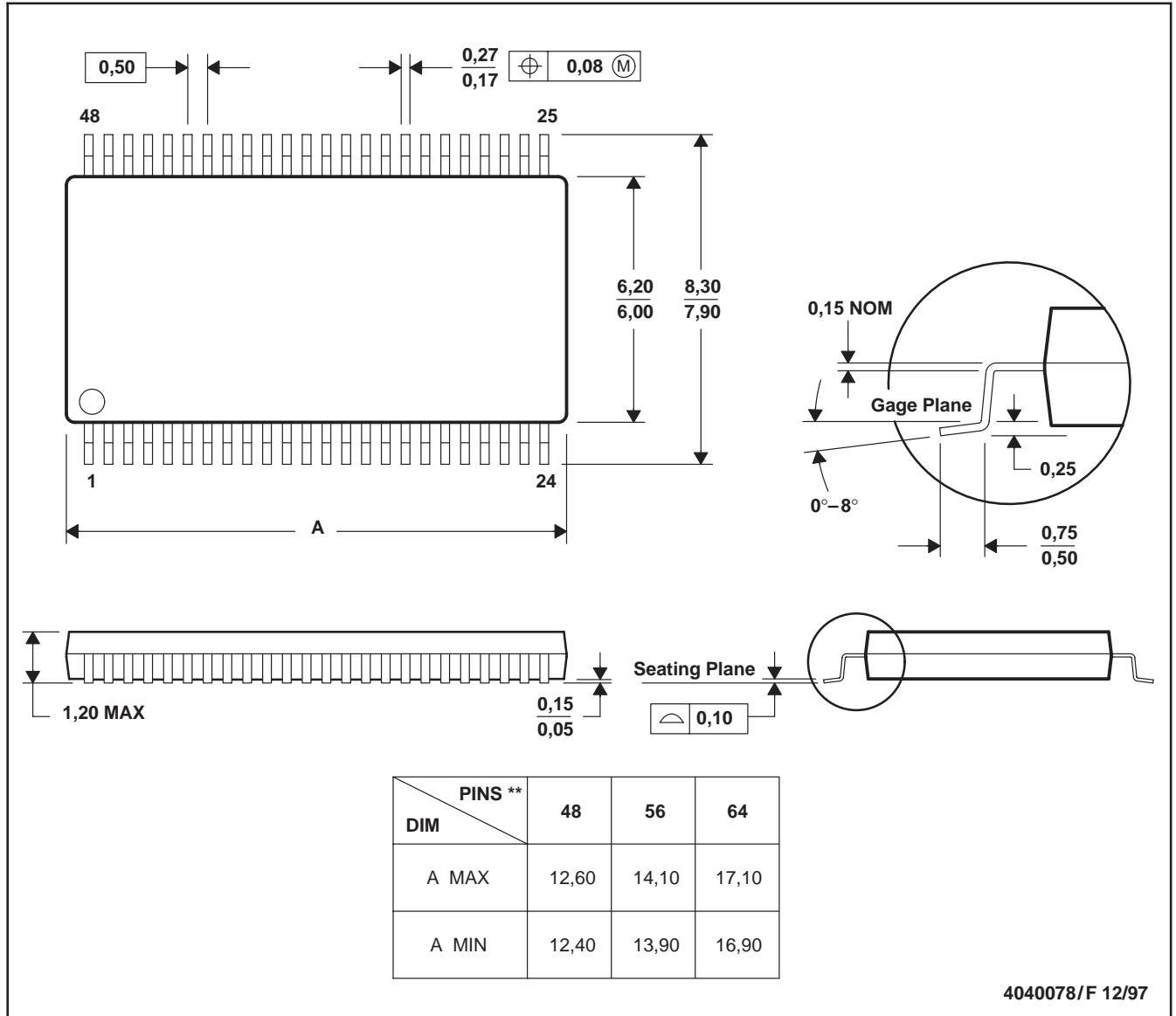


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

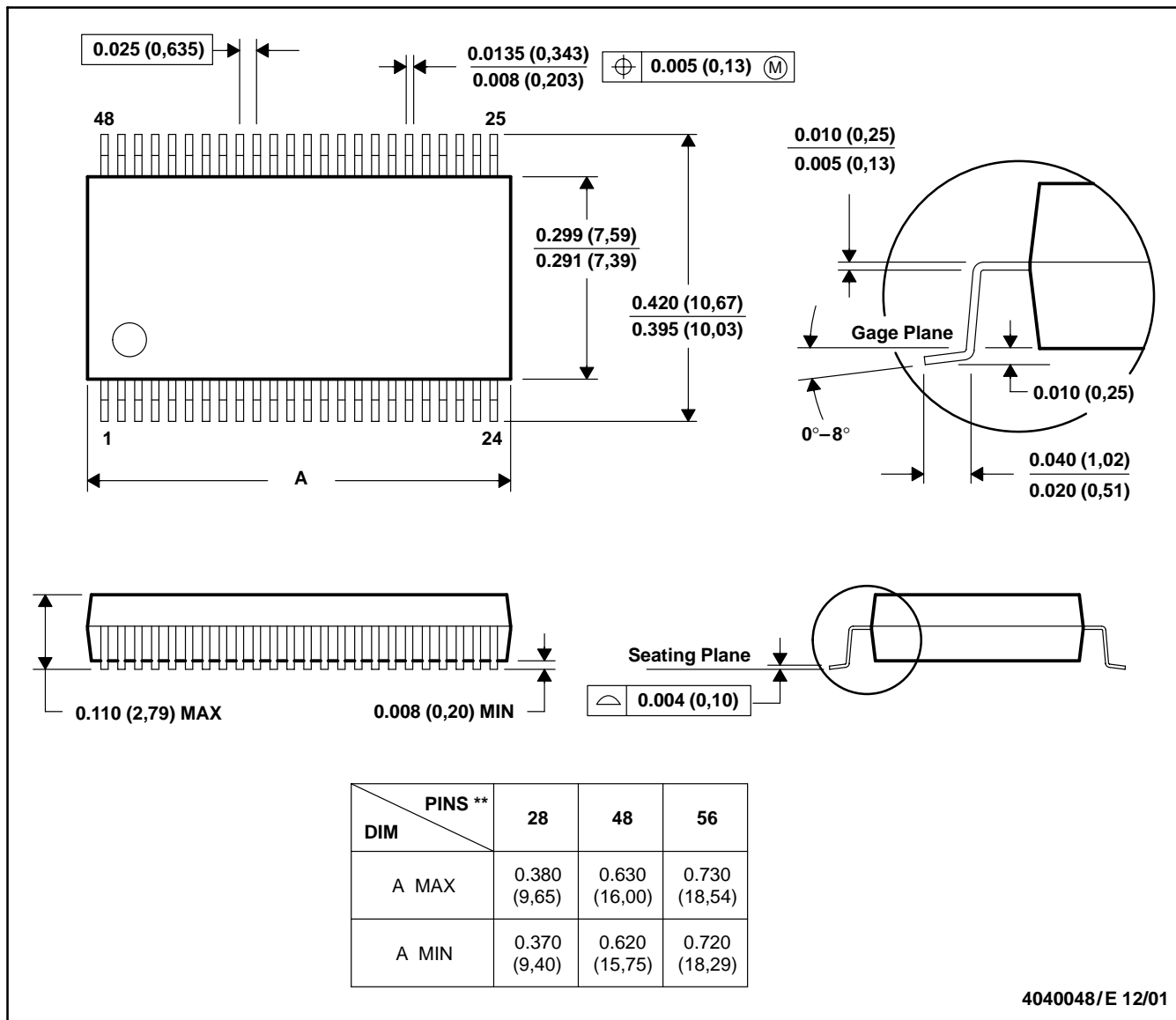


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

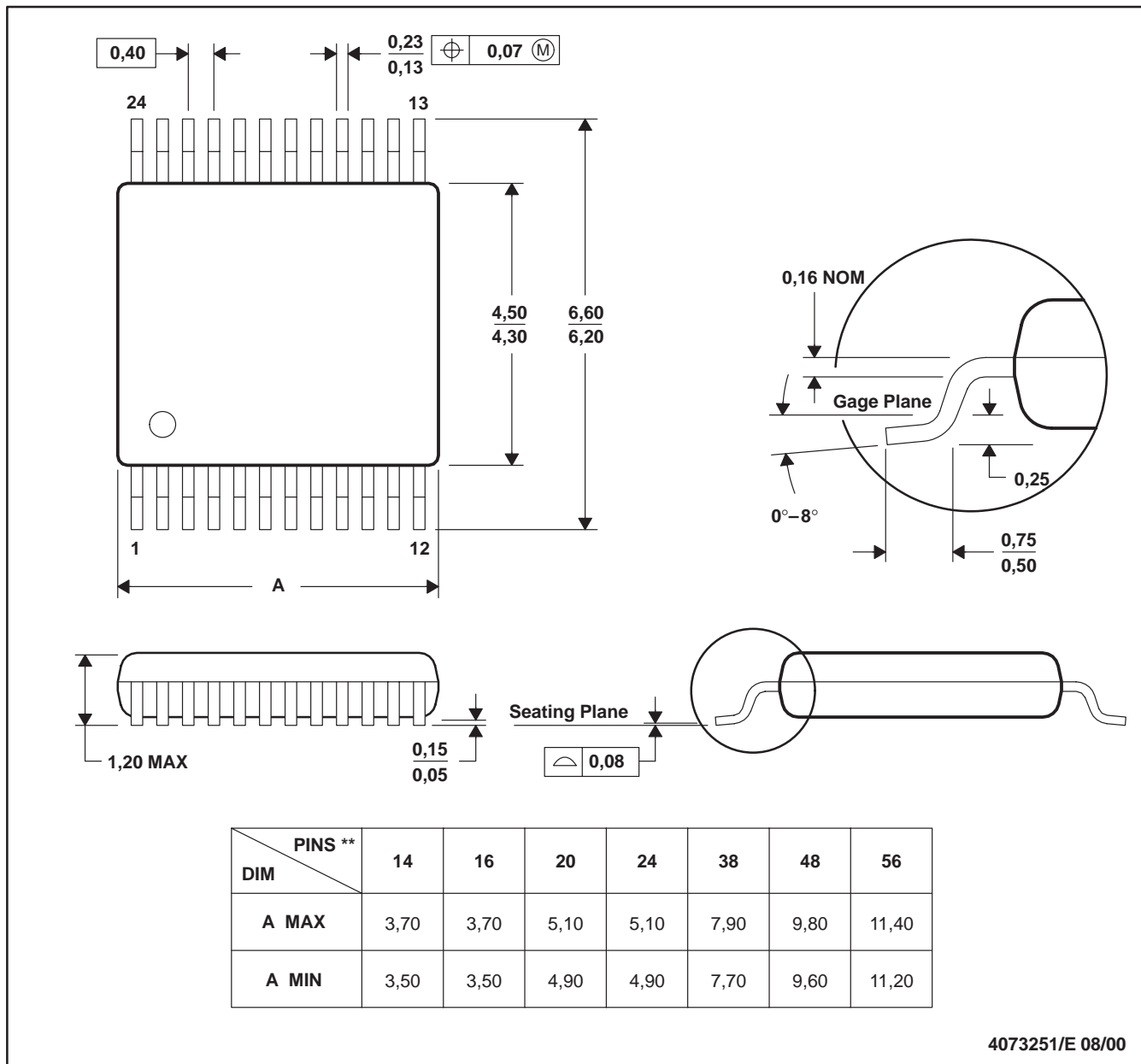


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

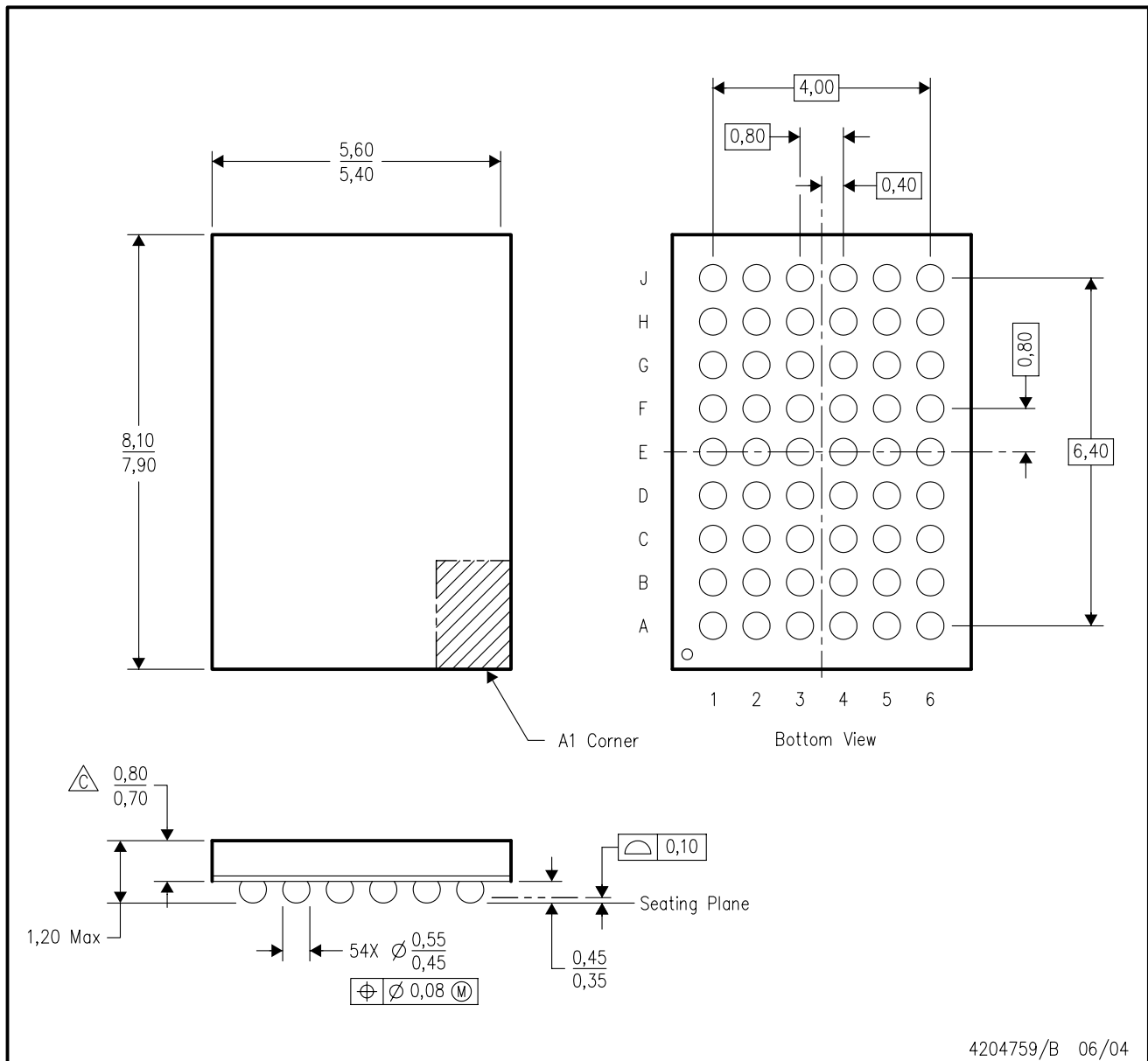
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GRD (R-PBGA-N54)

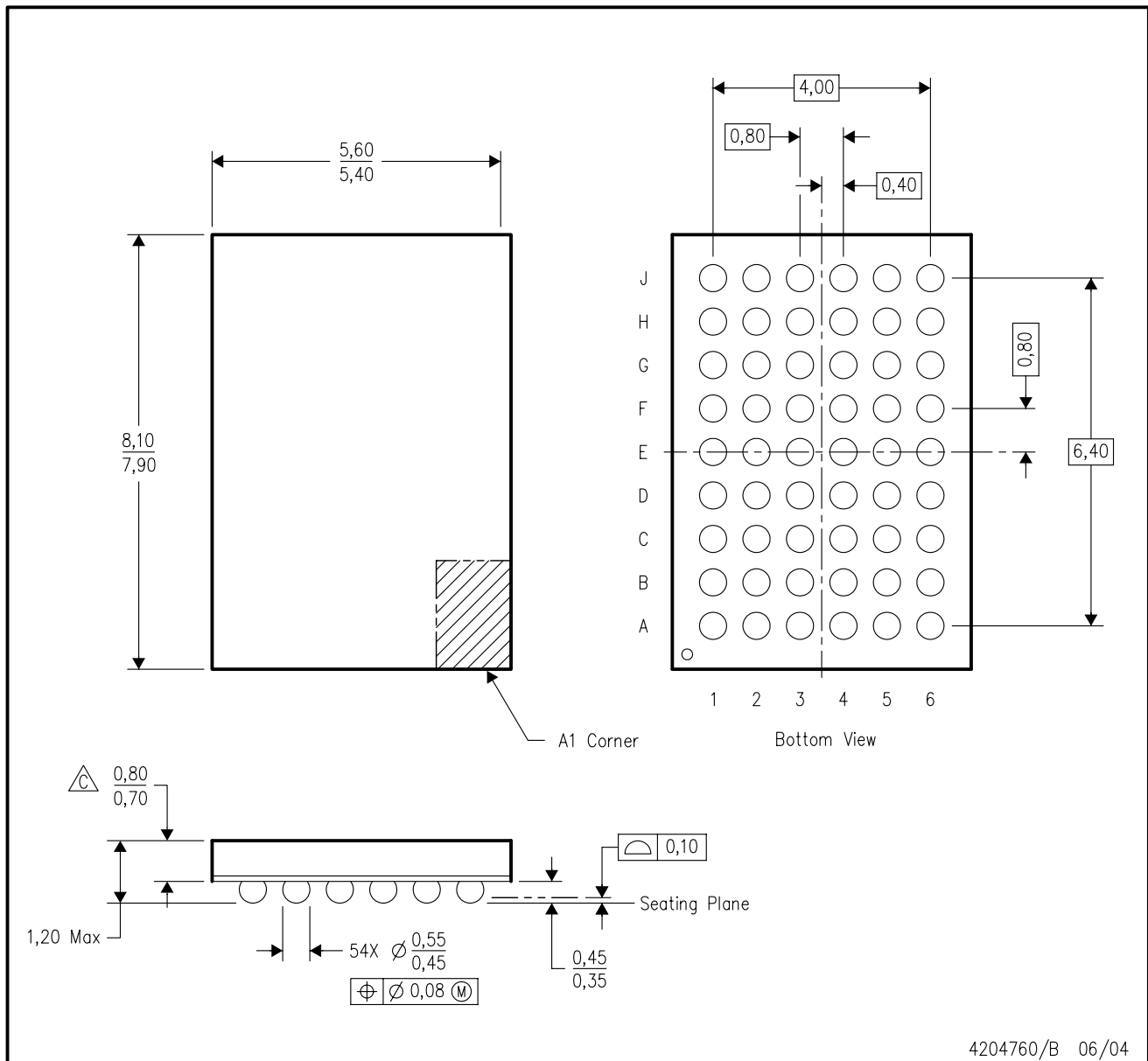
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MO-205 variation DD.
 - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MO-205 variation DD.
 - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

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